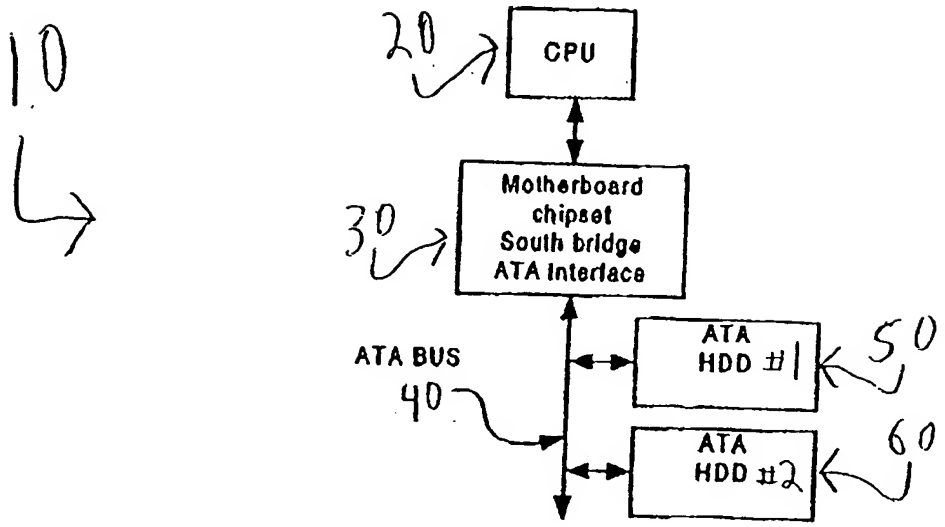


FIGURE 1
(PRIOR ART)

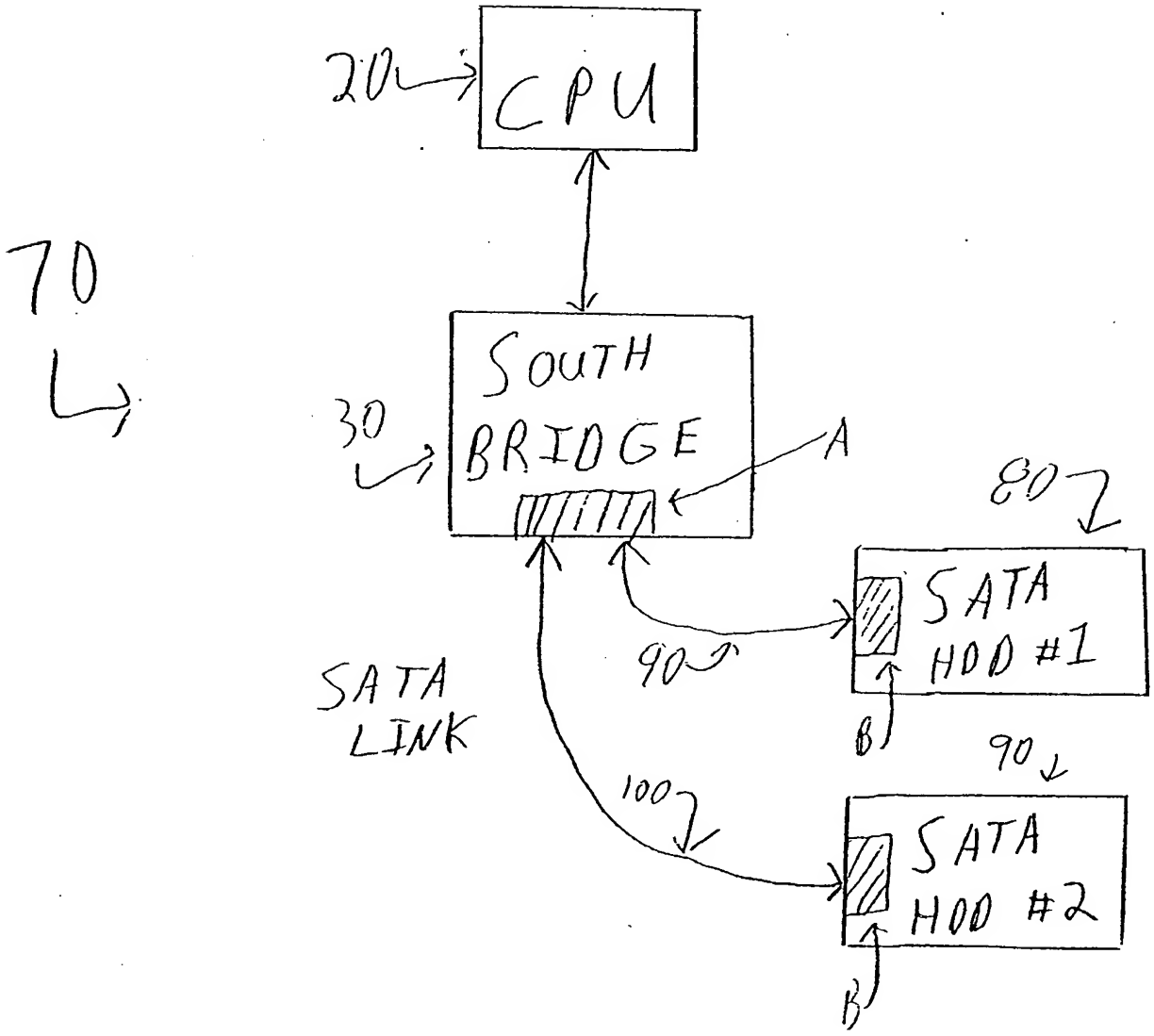


FIGURE 2
SATA LINKED SYSTEM
(PRIOR ART)

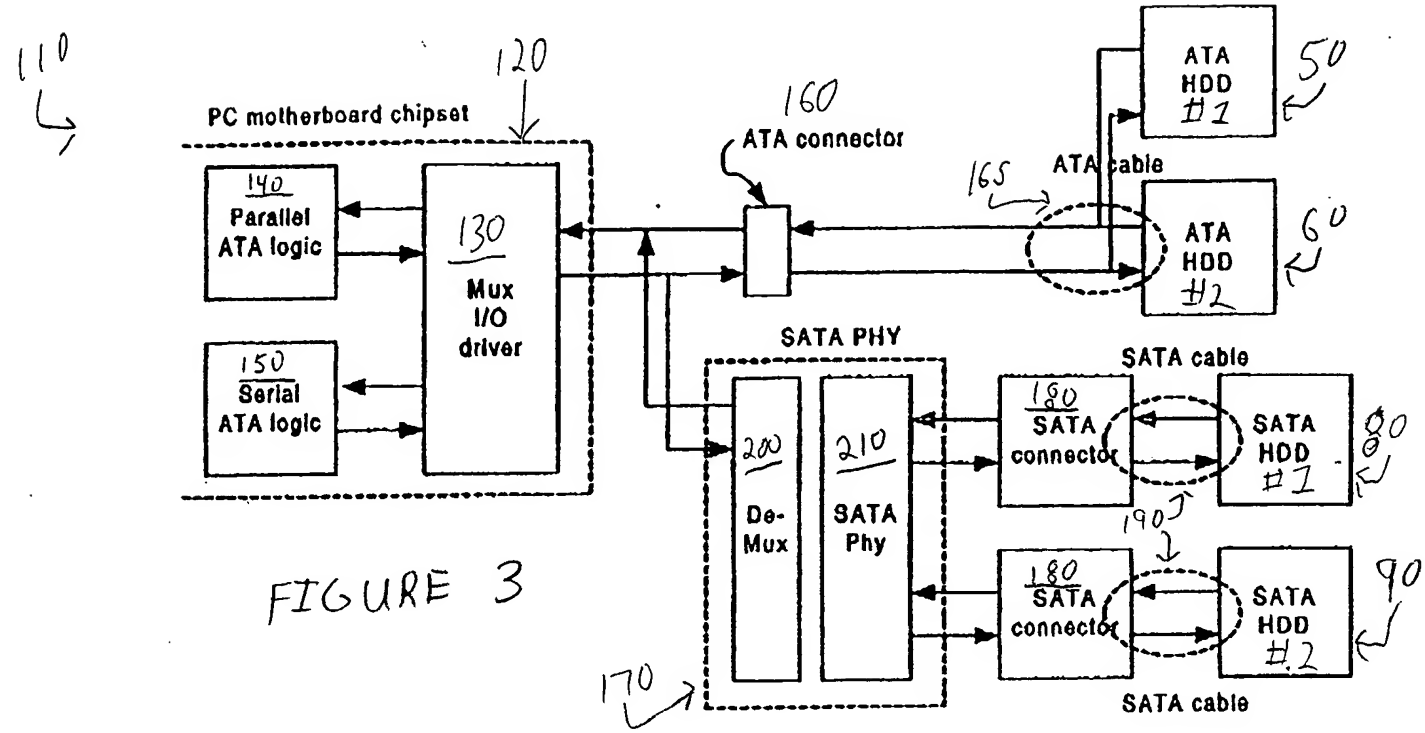


FIGURE 3

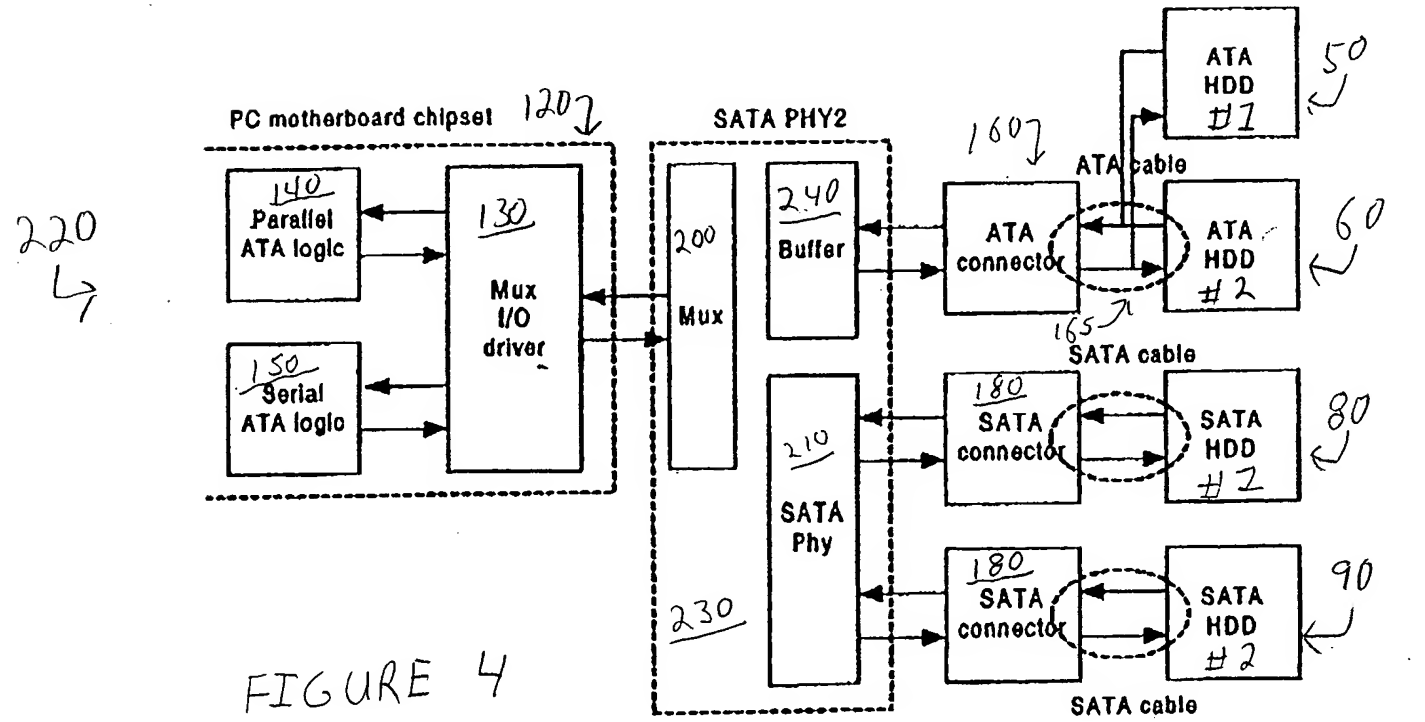


FIGURE 4

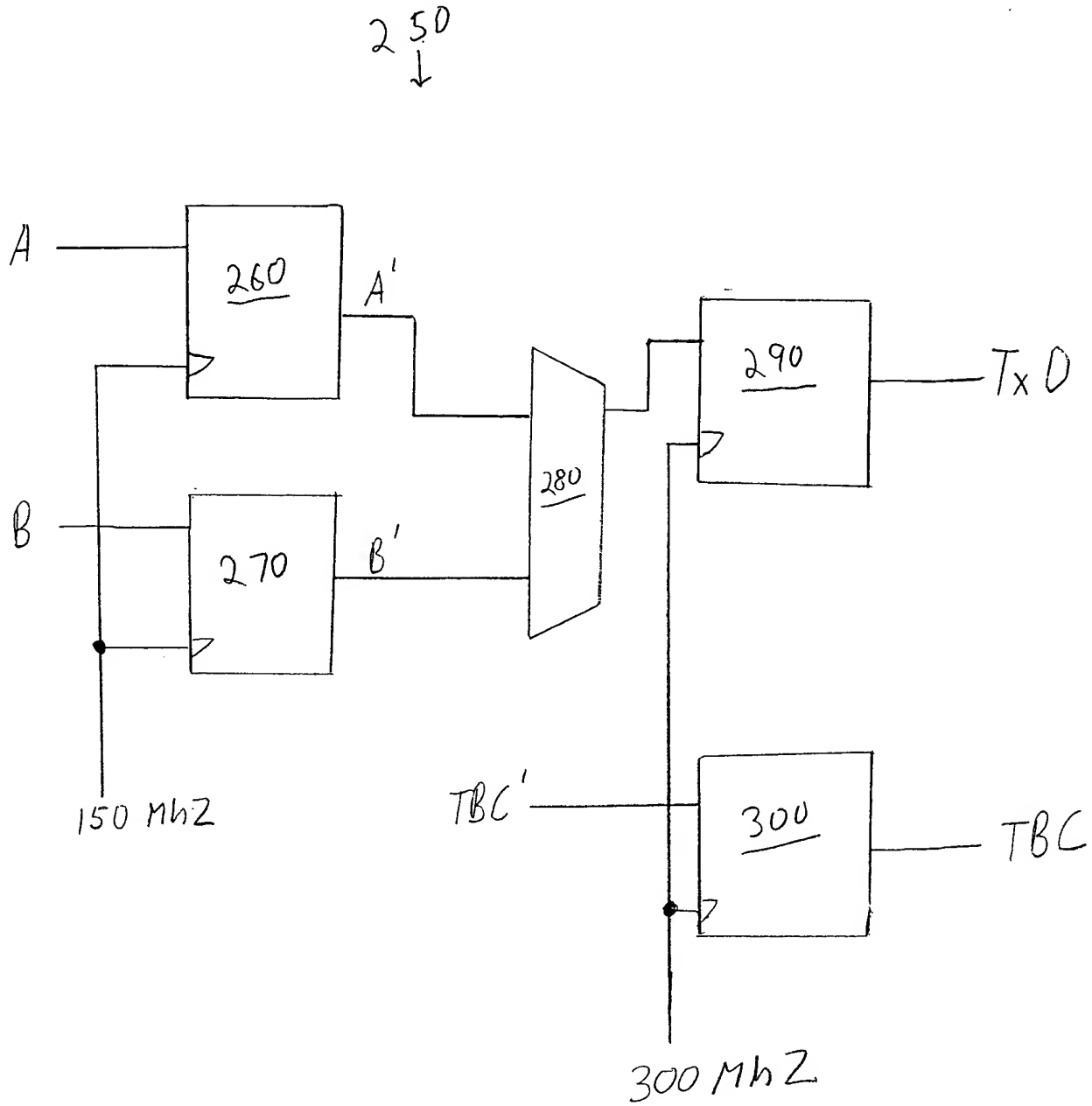
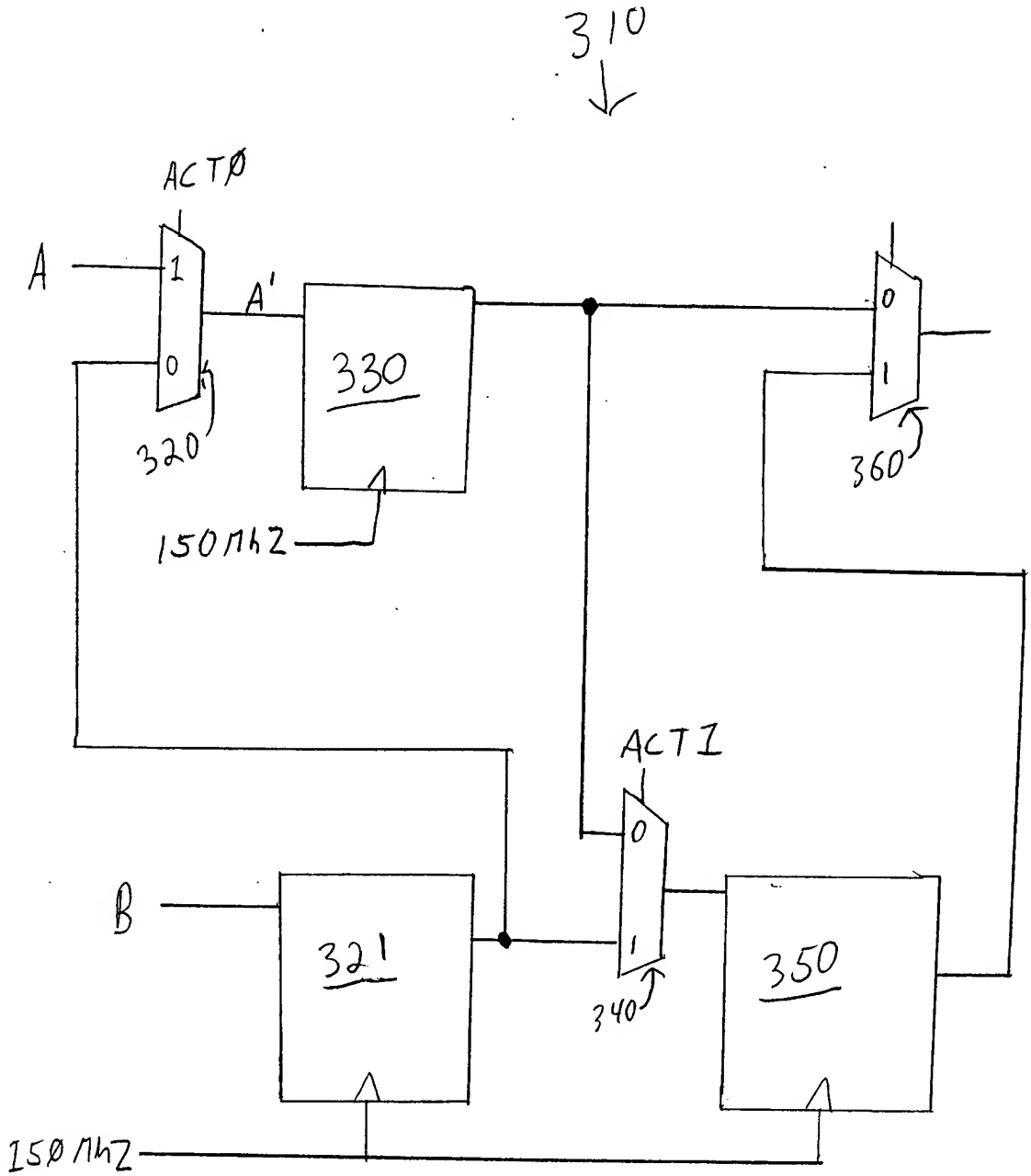


FIGURE 5A



ACT0	ACT1	
1	1	double data rate
0	1	single data rate
1	0	single data rate

FIGURE 5B

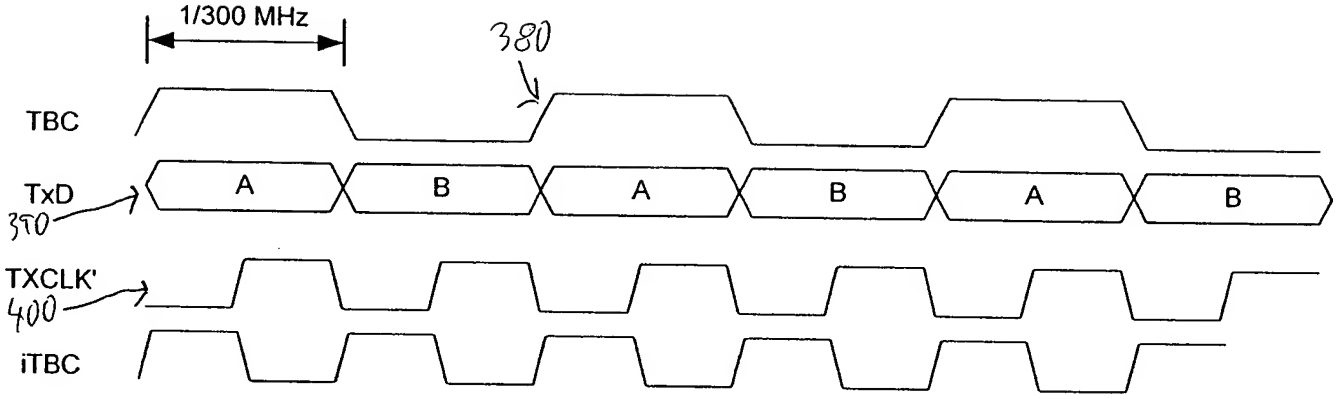


FIGURE 5C

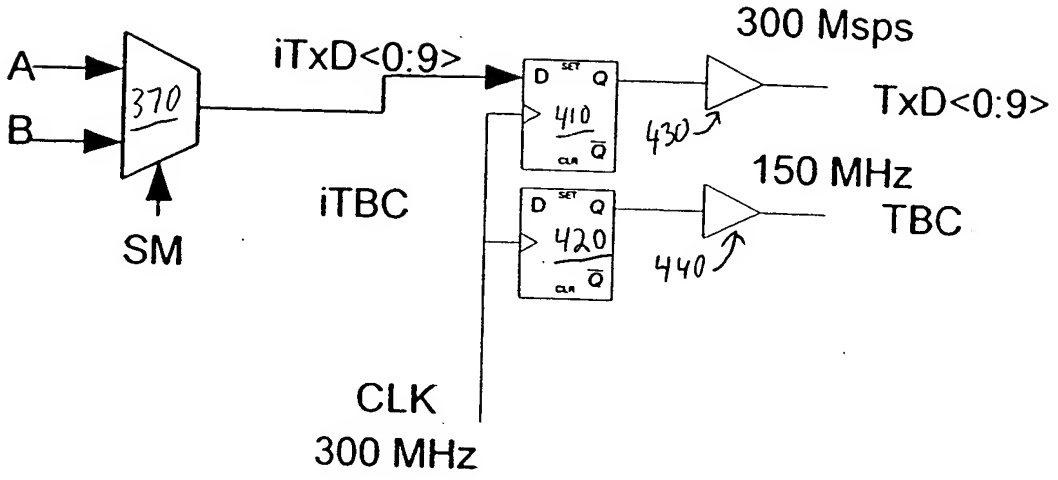

A
B
370
SM
iTxD<0:9>
iTBC
D SET Q
410
CLR Q̄
D SET Q
420
CLR Q̄
430
440
300 Msps
TxD<0:9>
150 MHz
TBC
CLK
300 MHz

FIGURE 6

170

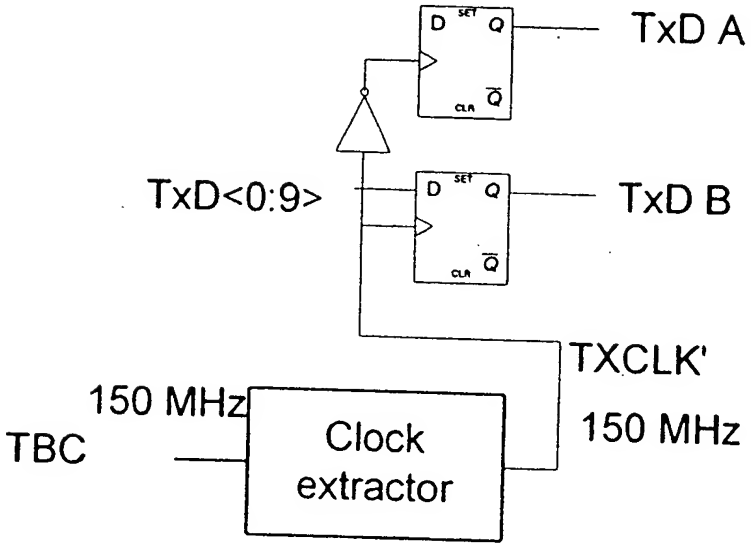

D
SET
Q
CLR
$\overline{Q}$
TxD A
TxD<0:9>
TxD B
TXCLK'
150 MHz
TBC
Clock extractor
150 MHz

FIGURE 7

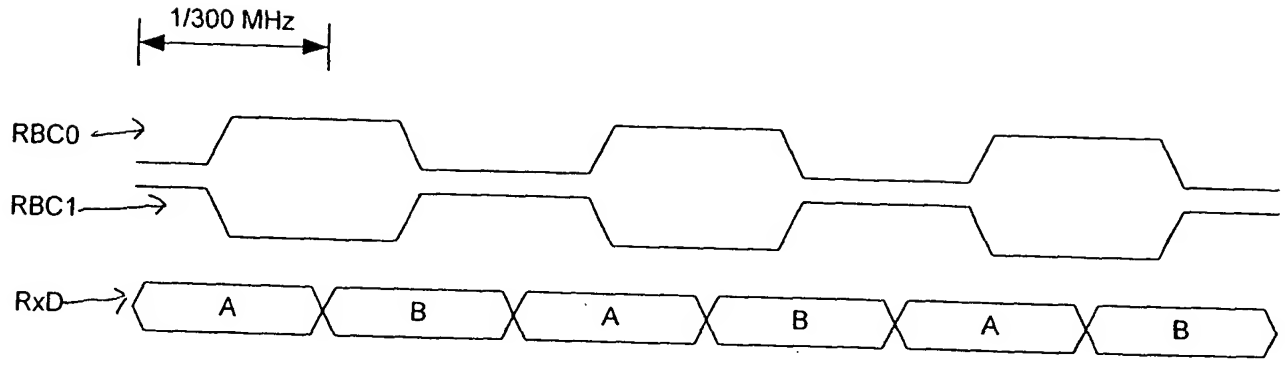


FIGURE 8

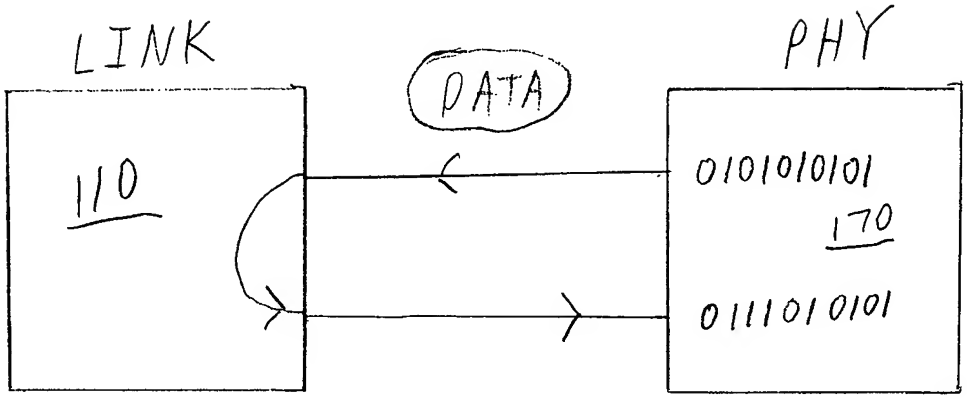


FIGURE 9A

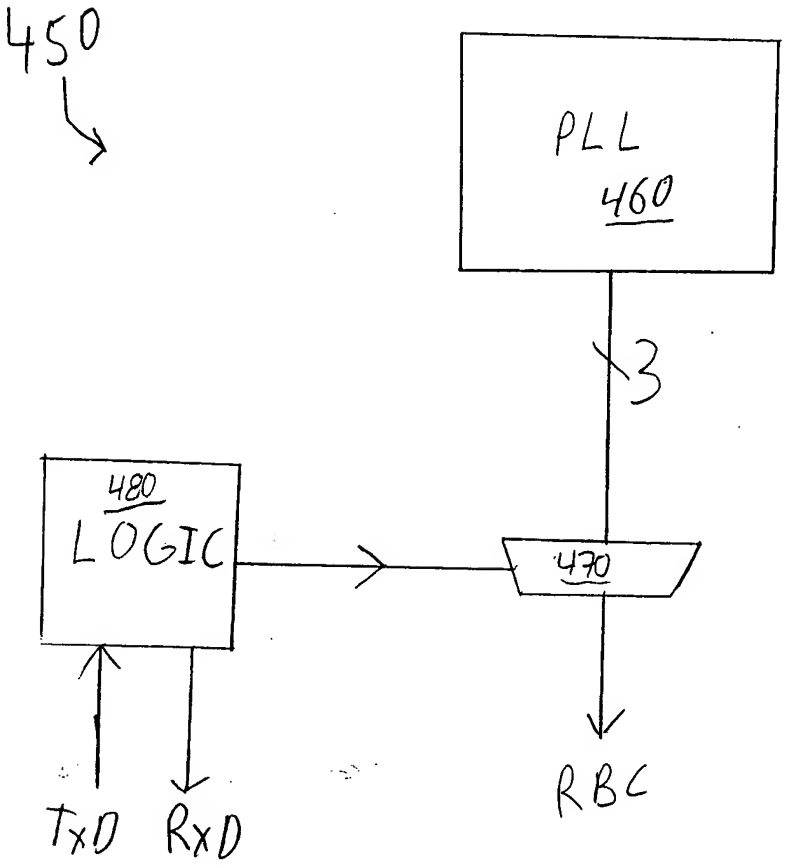


FIGURE 9B

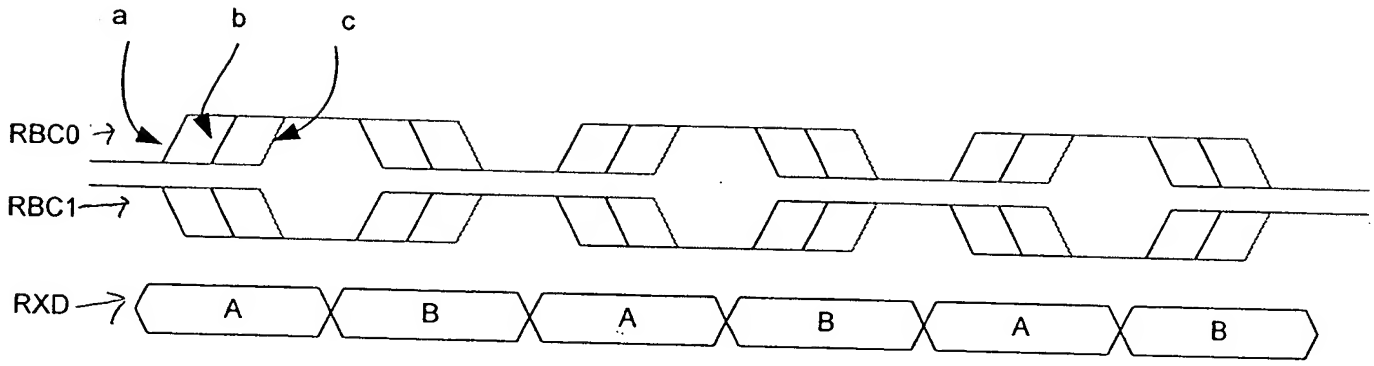


FIGURE 9C

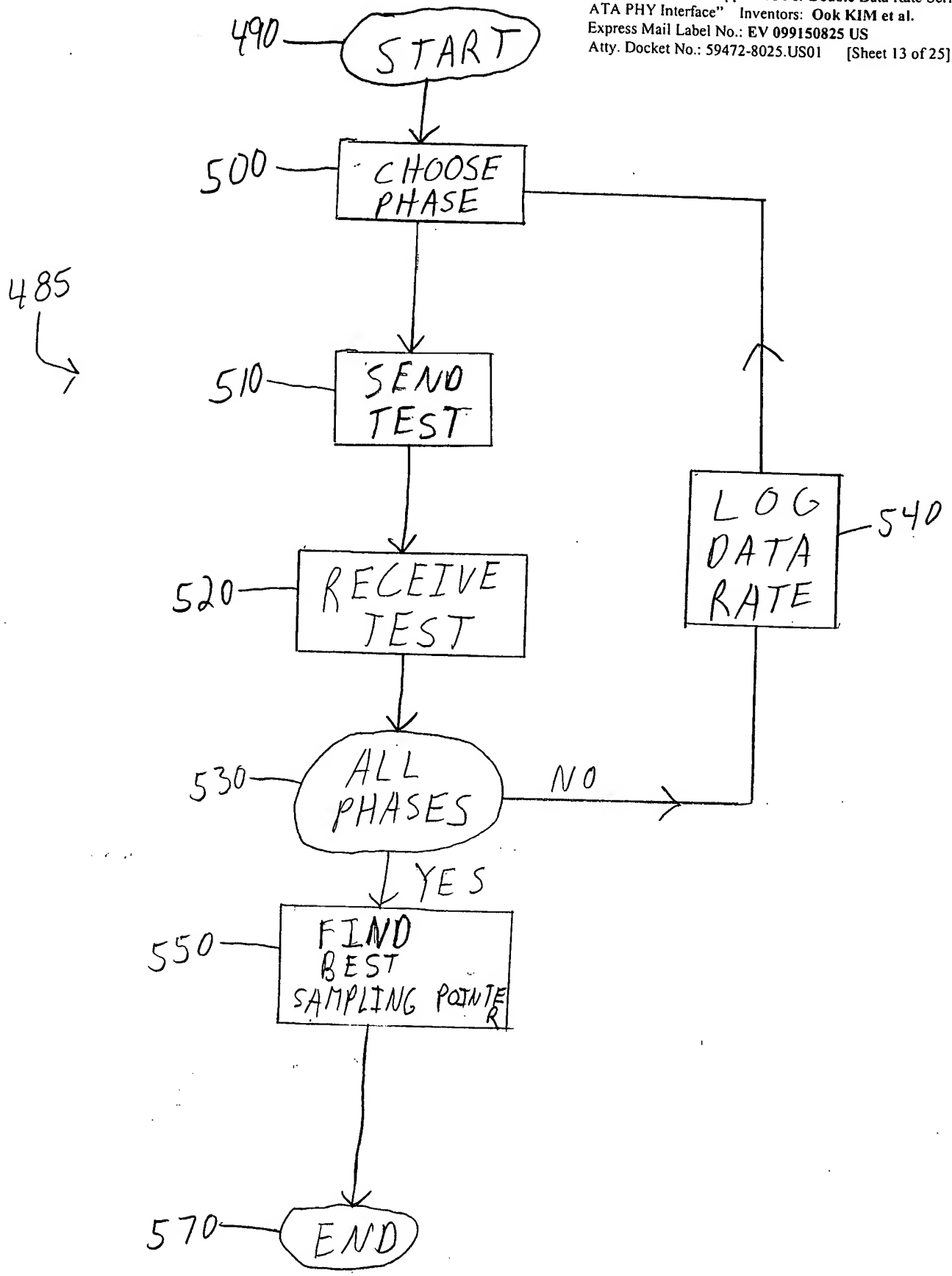

490
START
500
CHOOSE PHASE
485
510
SEND TEST
520
RECEIVE TEST
530
ALL PHASES
NO
YES
540
LOG DATA RATE
550
FIND BEST SAMPLING POINTER
570
END

FIGURE 10

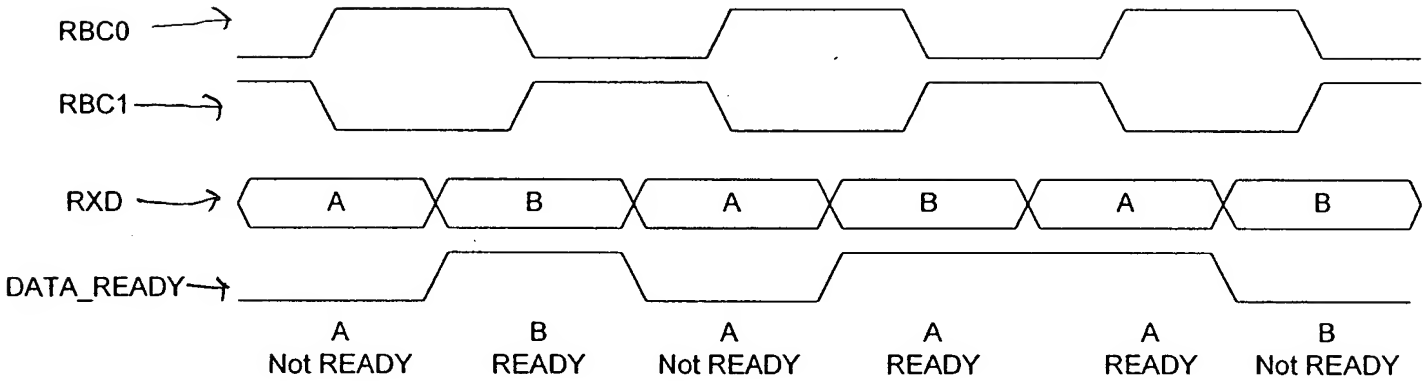

RBC0
RBC1
RXD
DATA_READY
A
B
A
B
A
B
A
Not READY
B
READY
A
Not READY
A
READY
A
READY
B
Not READY

FIGURE 11

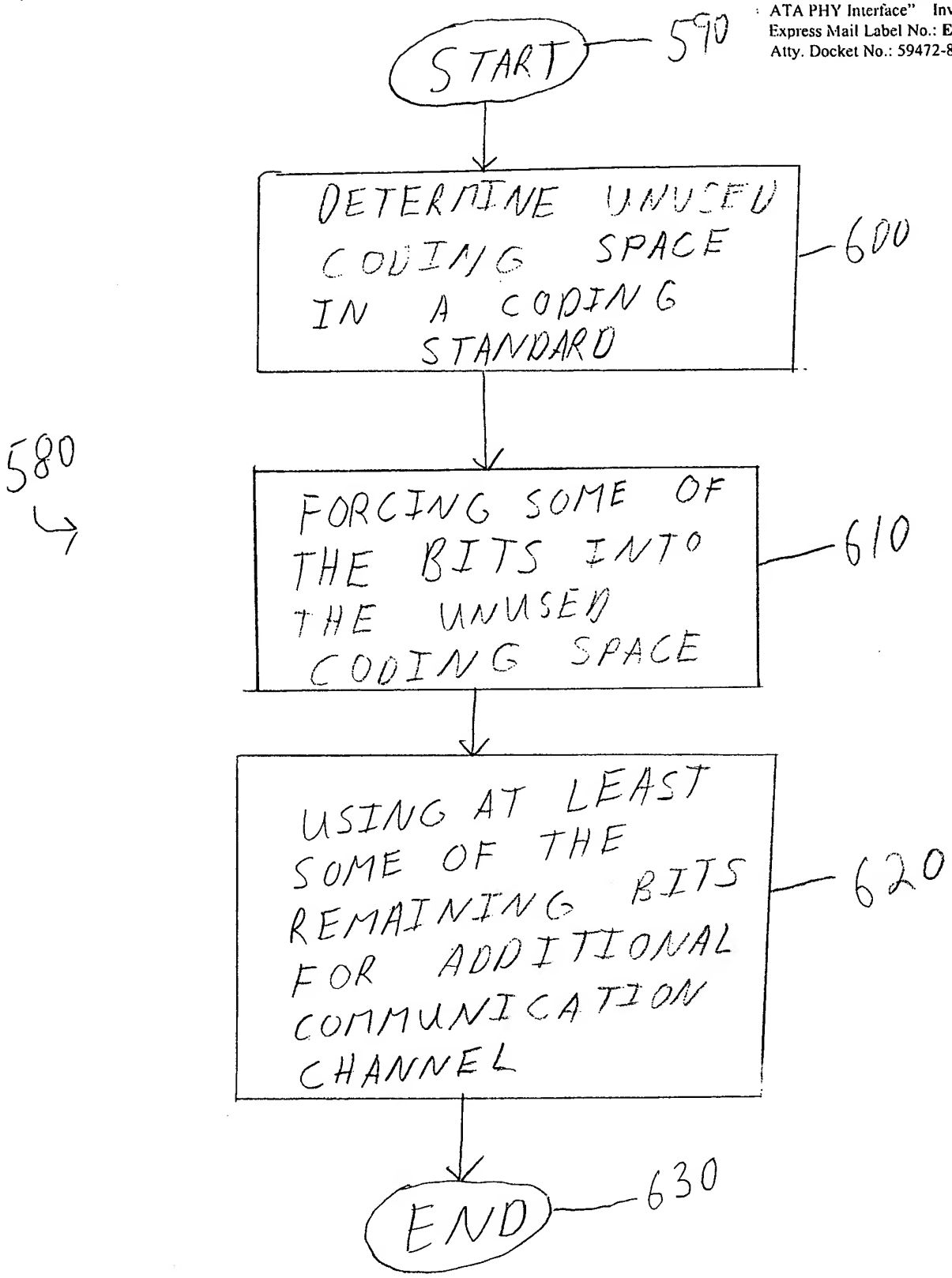

START
590
DETERMINE UNUSED CODING SPACE IN A CODING STANDARD
600
580
FORCING SOME OF THE BITS INTO THE UNUSED CODING SPACE
610
USING AT LEAST SOME OF THE REMAINING BITS FOR ADDITIONAL COMMUNICATION CHANNEL
620
END
630

FIGURE 12

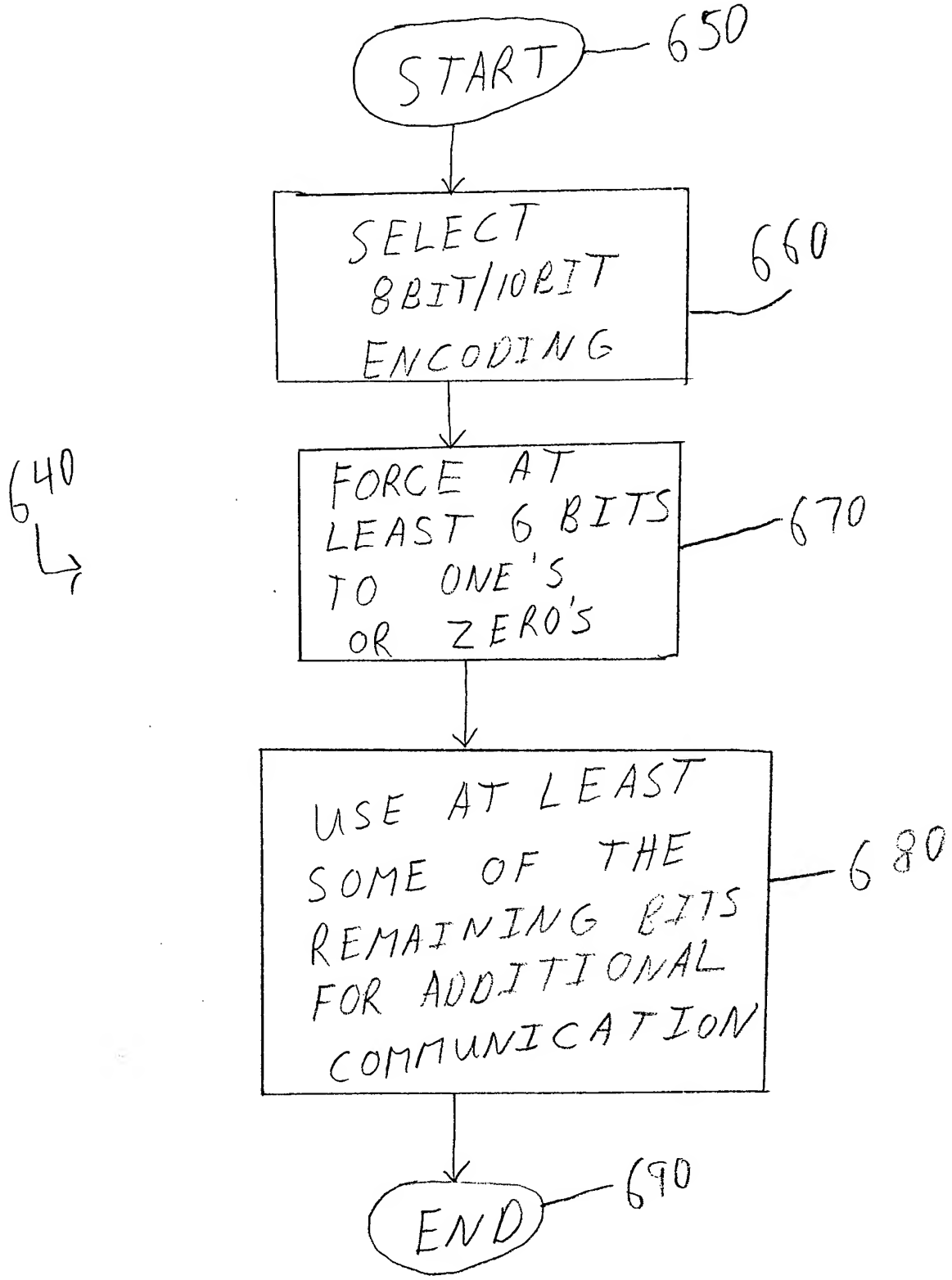

START
650
SELECT 8BIT/10BIT ENCODING
660
640
FORCE AT LEAST 6 BITS TO ONE'S OR ZERO'S
670
USE AT LEAST SOME OF THE REMAINING BITS FOR ADDITIONAL COMMUNICATION
680
END
690

FIGURE 13A

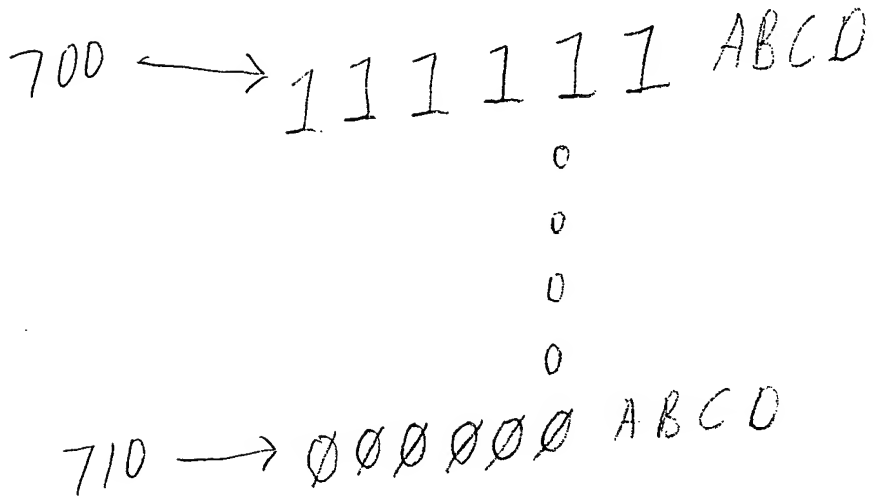


FIGURE 13B

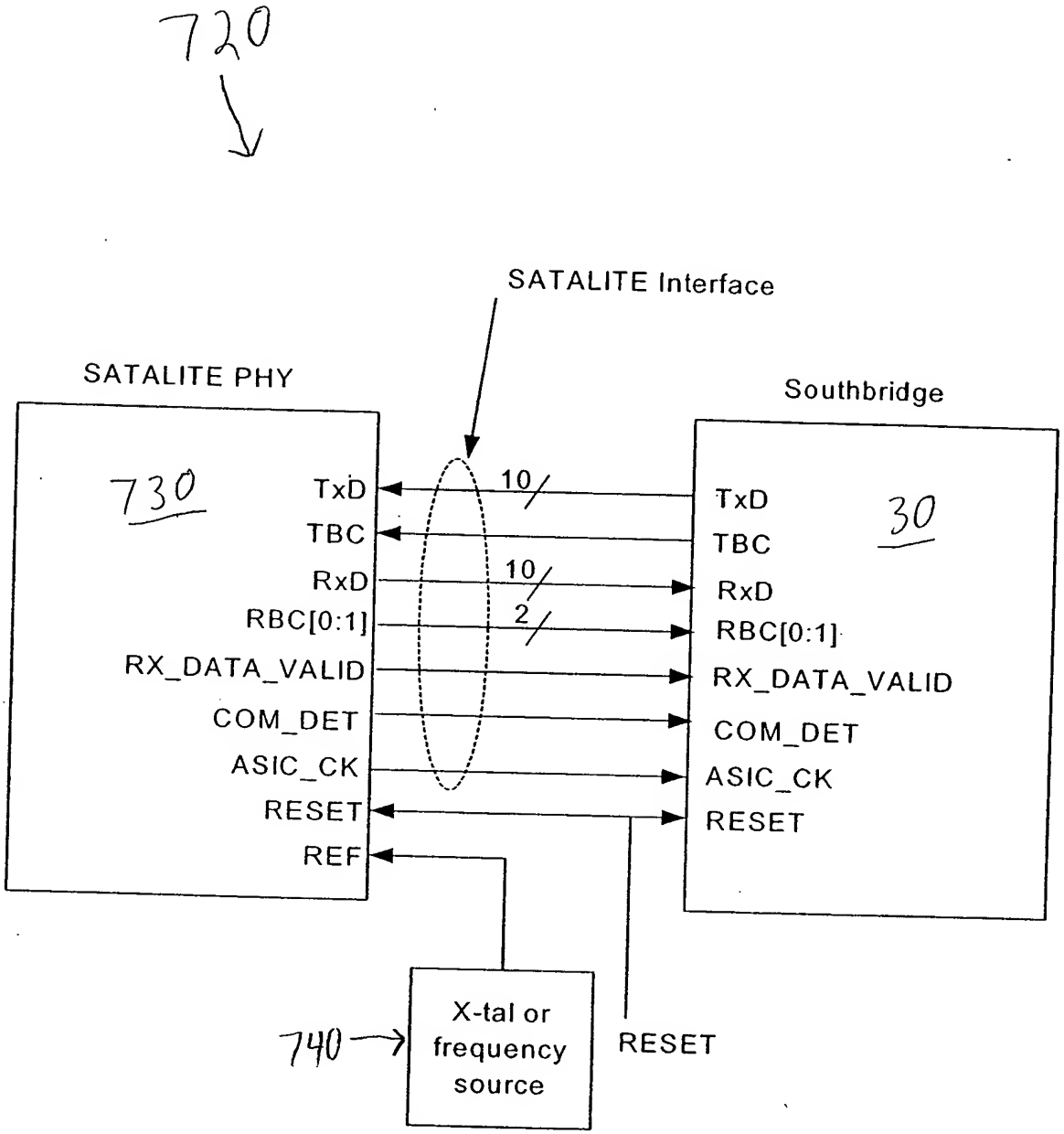

720
SATALITE Interface
SATALITE PHY
730
Southbridge
30
TxD
TBC
RxD
RBC[0:1]
RX_DATA_VALID
COM_DET
ASIC_CK
RESET
REF
10
10
2
TxD
TBC
RxD
RBC[0:1]
RX_DATA_VALID
COM_DET
ASIC_CK
RESET
740
X-tal or frequency source
RESET

FIGURE 14

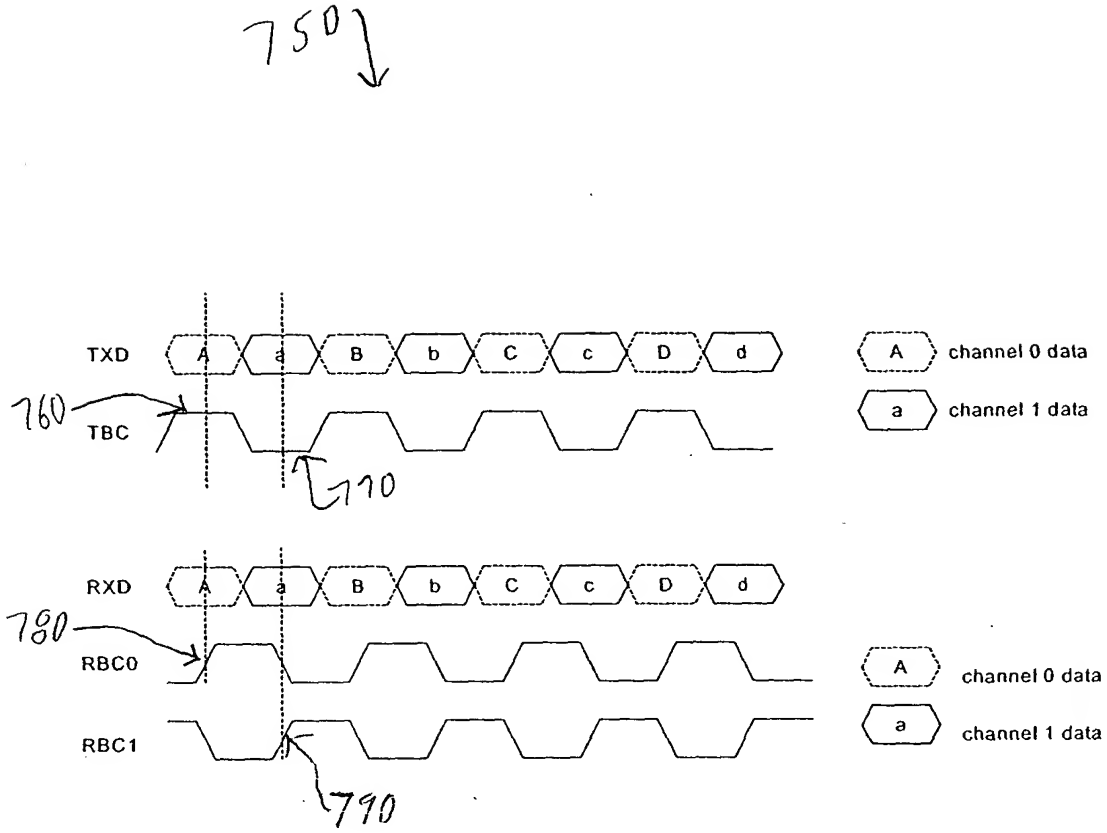

750
TXD
A
a
B
b
C
c
D
d
760
TBC
770
A channel 0 data
a channel 1 data
RXD
780
RBC0
RBC1
790

FIGURE 15

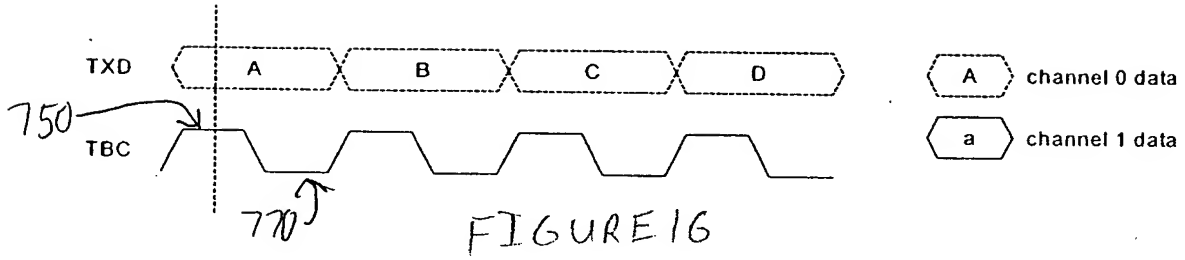


FIGURE 16

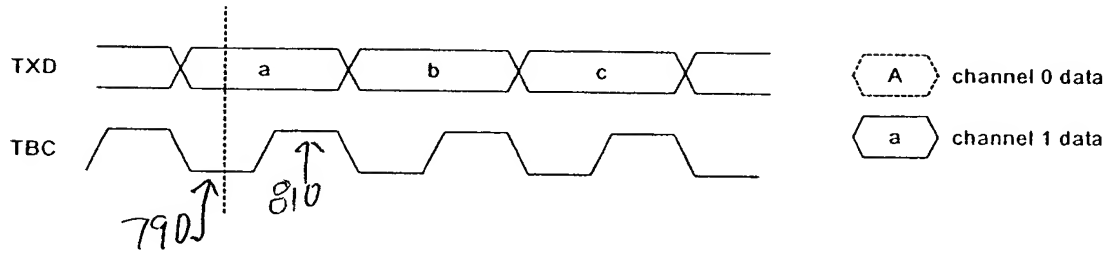


FIGURE 17

FIGURE 18

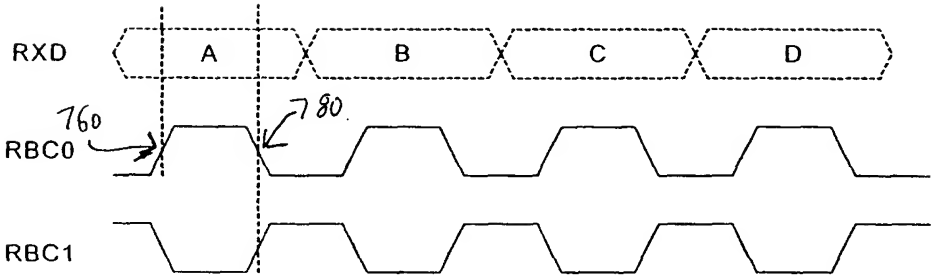
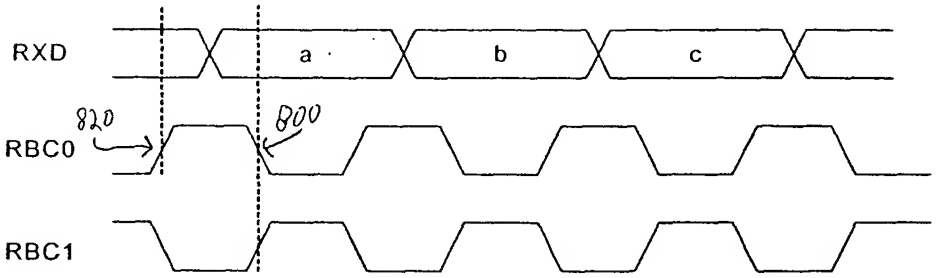


FIGURE 19



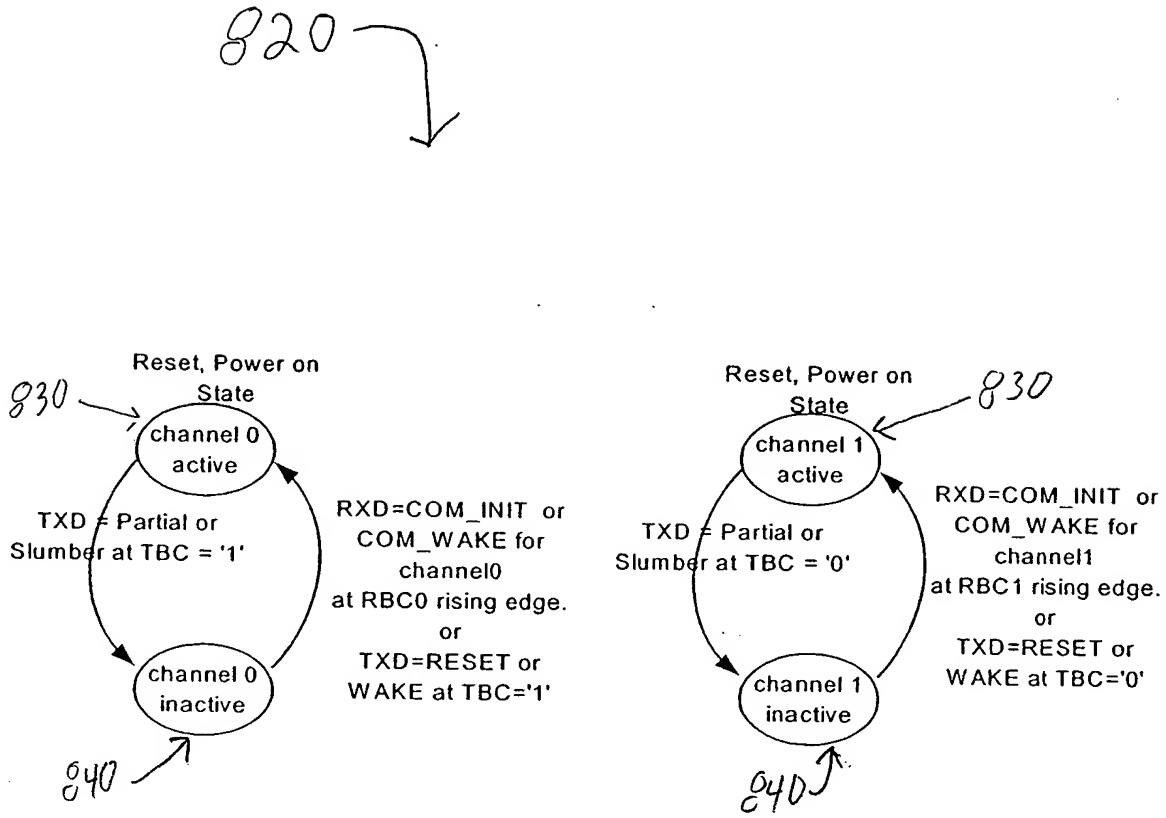

820
830
Reset, Power on State
channel 0 active
TXD = Partial or Slumber at TBC = '1'
RXD=COM_INIT or COM_WAKE for channel0 at RBC0 rising edge. or TXD=RESET or WAKE at TBC='1'
channel 0 inactive
840
Reset, Power on State
830
channel 1 active
TXD = Partial or Slumber at TBC = '0'
RXD=COM_INIT or COM_WAKE for channel1 at RBC1 rising edge. or TXD=RESET or WAKE at TBC='0'
channel 1 inactive
840

FIGURE 20

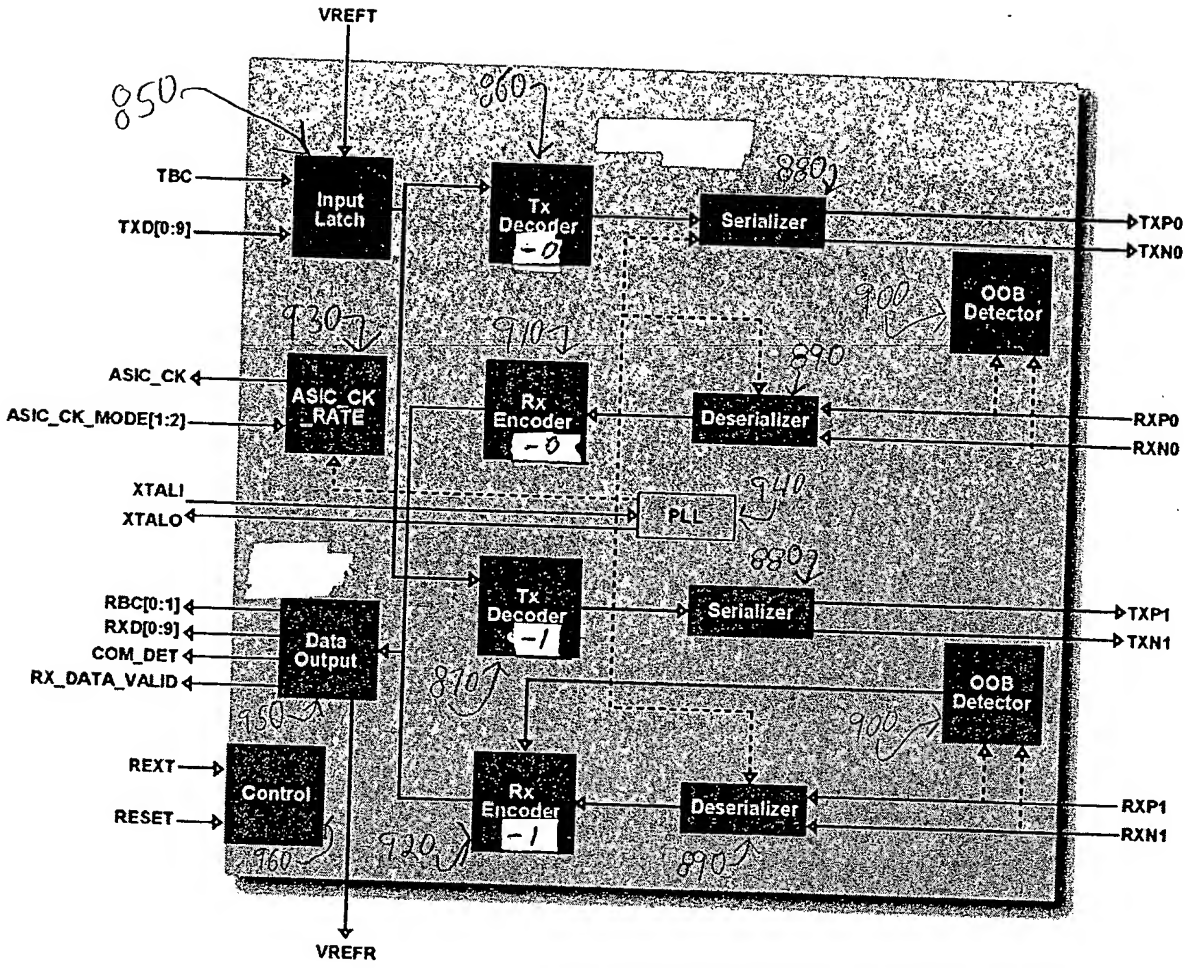

730
VREFT
850
860
TBC
TXD[0:9]
Input Latch
Tx Decoder -0
880
Serializer
TXP0
TXN0
OOB Detector
900
930
910
890
ASIC_CK
ASIC_CK_MODE[1:2]
ASIC CK _RATE
Rx Encoder -0
Deserializer
RXP0
RXN0
XTALI
XTALO
PLL
940
Tx Decoder -1
Serializer
TXP1
TXN1
RBC[0:1]
RXD[0:9]
COM_DET
RX_DATA_VALID
Data Output
OOB Detector
REXT
RESET
Control
Rx Encoder -1
Deserializer
RXP1
RXN1
950
960
920
VREFR

FIGURE 21

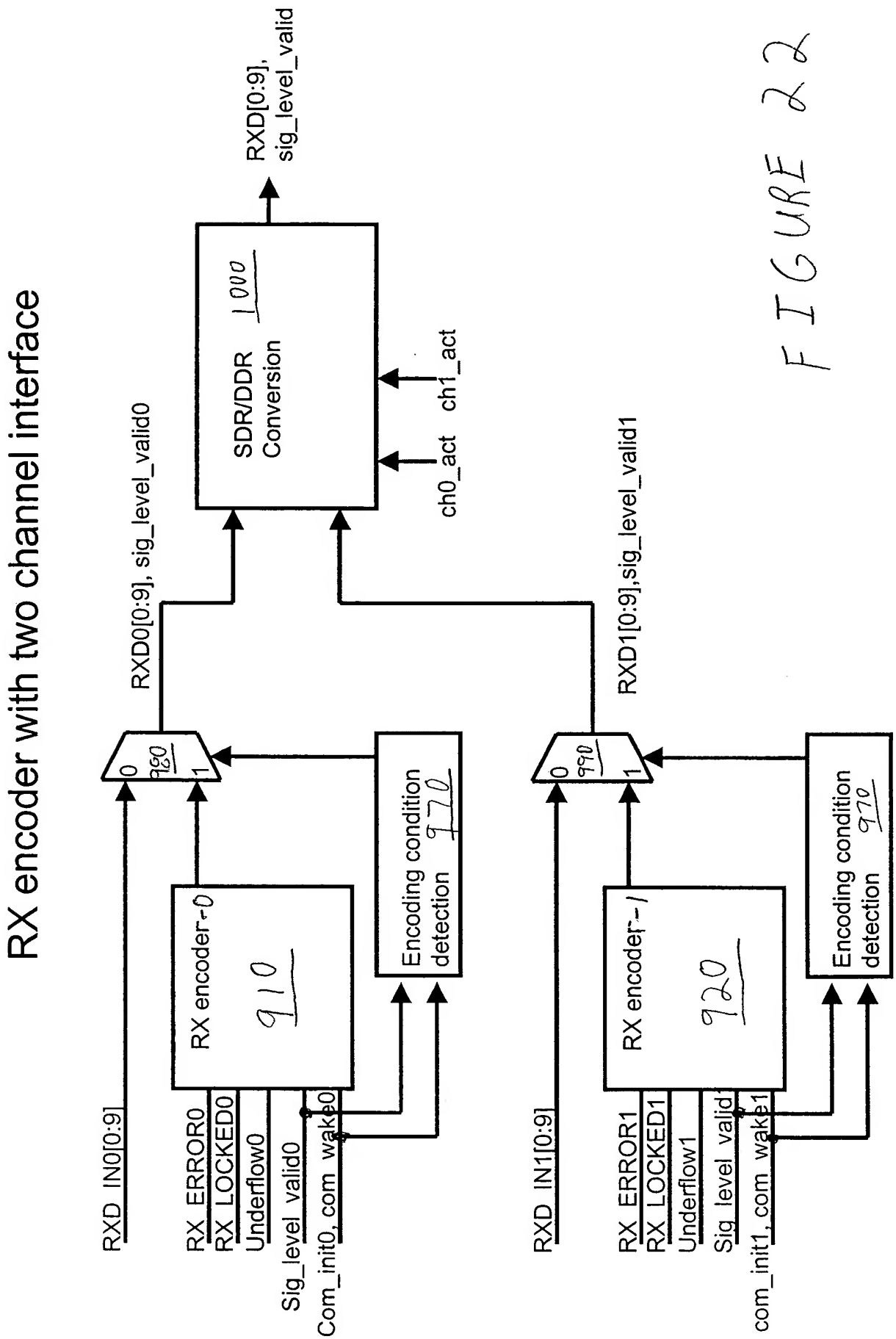

RX encoder with two channel interface
RXD[0:9], sig_level_valid
SDR/DDR Conversion 1000
RXD0[0:9], sig_level_valid0
RXD1[0:9],sig_level_valid1
ch0_act
ch1_act
0
960
1
0
990
1
RX encoder-0 910
RX encoder-1 920
Encoding condition detection 970
Encoding condition detection 970
RXD_IN0[0:9]
RXD_IN1[0:9]
RX_ERROR0
RX_LOCKED0
Underflow0
Sig_level_valid0
Com_init0, com_wake0
RX_ERROR1
RX_LOCKED1
Underflow1
Sig_level_valid1
com_init1, com_wake1

FIGURE 22

FIGURE 23A

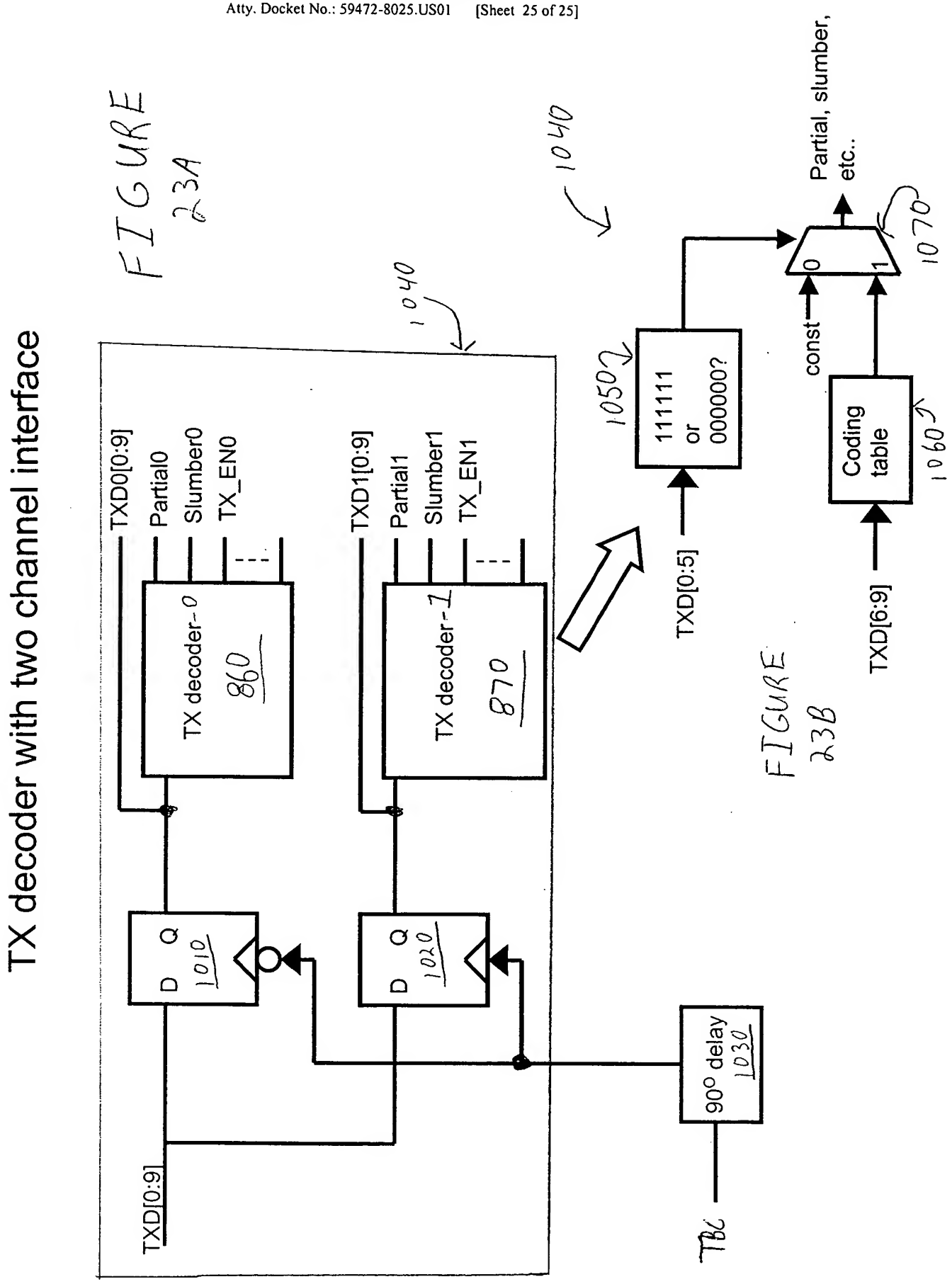


FIGURE 23B